REMARKS

Claims 1-7 were pending. Claim 5 has been canceled herein. Thus, claims 1-4, 6, and 7 are now pending. The applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all of the certified copies of the priority documents have been received.

The applicants acknowledge and appreciate receiving an initialed copy of the form PTO-1449 which accompanied the Information Disclosure Statement that was filed on March 4, 2004 and June 7, 2005.

Claims 1, 2, 6, and 7 were objected to because the preamble and body are not clearly recited. The claims are amended herein to address the objection.

Claims 1-7 were rejected under 35 USC 112, second paragraph, as being allegedly indefinite. Without acknowledging the propriety of the rejection, the claims have been amended herein to address matters of form and clarity only and not for reasons related to patentability.

With the exception of the minor antecedent basis issues, the Examiner primarily states that it is not understood how certain elements function or what they are. This is not the test for establishing a proper *prima facie* case of indefiniteness. The primary test of indefiniteness is whether one of ordinary skill in the art when reading the claims in light of the specification would have understood the claims *with a **reasonable** degree of certainty.* An objection would have been a more appropriate manner to address the matters of form such as the antecedent basis issues.

With regard to the structure of the circuit or whether or not the circuit provides an output, applicants are not aware of a requirement, particularly under 35 U.S.C. 112 2nd paragraph that a claimed structure perform any specific function such as providing an output or have a certain connection so long as the claim meets basic requirements such as, for example, the subject matter requirements of 35 U.S.C. 101 or the written description requirements of 35 U.S.C. 112 1st paragraph. Although no rejection under 35 U.S.C. 101 or 35 U.S.C. 112 1st paragraph has been applied, applicants submit that the claims clearly meet basic subject matter requirements and are adequately enabled in that one of ordinary skill in the art would, given the description and figures provided in the applicants specification, be able to make and use the invention.

With regard to questions of "what" certain features are or "how" they work, the applicants are not aware of a requirement to provide a detailed explanation of how the claimed invention works. Again, applicants contend that the test for definiteness is whether one of ordinary skill would have understood the claims with a reasonable degree of certainty. However, applicants submit that, for example, with regard to the Examiner's question as to what the "predetermined maximum operating temperature" is in claim 3, one of ordinary skill could consult page 26, lines 1 to 11 of the specification to understand the relevance of the claimed temperature, which one of ordinary skill in the art would appreciate need not be recited with a specific numerical value as the maximum operating temperature may differ without affecting the meaning of the claimed feature. Similarly, questions regarding the range of time interval values can be addressed, for example, with reference to page 26, line 17, questions regarding DC error percentages can be found on page 27, line 3, and questions regarding stored charge can be found on 27, line 7-10 of applicants' specification.

However, to expedite prosecution and improve the clarity thereof, the claims have been amended to the extent necessary to address issues of clarity only and not for reasons related to

patentability. Thus, the scope of the claims for the purposes of the application of the doctrine of equivalents has not been affected.

Claims 1-7 were rejected under 35 USC 103(a) as being allegedly unpatentable over Figure 7 of the applicants' allegedly admitted prior art. The applicants respectfully request that this rejection be withdrawn for the following reasons.

In making the rejection, the Examiner has asserted that it would have been a mere design expedient for a person skilled in the art to select the optimum duration of the switching conditions for the switching elements described for example, in figures 7 and 8 of the present application for the purpose of optimizing the filtering function and accommodating the requirements of a particular system.

Applicants note that, although various systems could benefit from a low-pass filter capable of having a very low value of cut-off frequency, and given that the use of switched capacitor filters have various advantages with respect to ease of manufacture, and the like, there has heretofore been no proposal in the art for constructing a switched capacitor filter having a very low value of cut-off frequency, particularly based on a known configuration, such as in Fig. 7 of the present application. The lack of suggestion or teaching in the art arises from the undesirable effects of leakage current within the switching elements of the filter which pose limits on the extent to which the cut-off frequency can be lowered. The lack of suggestion is, in itself, an expression of a long felt need and the criticality of the operations conducted in accordance with the claimed invention are expressed in connection with the problems encountered in the prior art as exhaustively described in the Description of Prior Art of the present application.

In the prior art, for example in a switched capacitor filter of the type shown in Fig. 7, e.g. one in which two sets of switching elements are respectively controlled by respective phases of a 2-phase clock signal, a condition periodically occurs in which all of the switching elements are set in the open-circuit condition. Such an open circuit condition is shown, for example, in the circuit diagram of Fig. 5B. The prior art effects of the condition are shown in the timing diagram of Figure 8 as the "phase 2" interval. Each phase 2 interval begins immediately after an input capacitor, e.g., C1, has been charged to a potential of a signal input to the filter. Immediately following each phase 2 interval, e.g., in the succeeding phase 3 interval, the charge held in the input capacitor is supplied to a pair of capacitors (C2, C3), which at the phase 3 time are connected in parallel between input and output terminals of the operational amplifier (OP1) of the filter as shown for example, in Fig. 5C. The applicants have found that if the amount of leakage of the charge held in the input capacitor (C1) during each phase 2 interval can be minimized, then a switched capacitor filter with a substantially lower cut-off frequency than has been possible in the prior art can be attained.

In order to minimize the amount of leakage of the charge held in the input capacitor (C1) through the switching elements connected to C1 during each phase 2 interval, the applicant proposes to reduce the duration of each phase 2 interval as far as possible. Specifically, the time that elapses between the end of the active status of a first clock signal phase e.g., the time at which the switches S11 and S25 connected to capacitor C1 are closed and opened respectively as shown in Fig. 5A of applicants' specification, and the start of the active phase of the second clock signal phase e.g., the time at which the switches S11 and S25 are opened and closed respectively as shown in Fig. 5C of applicants' specification, is made as short as possible. In particular, the duration of each phase 2 interval should be such that the amount of leakage of charge from the input capacitor (C1) during that interval, expressed as a percentage of the initial

amount of charge at the start of the interval, should be no greater than the maximum permissible amount of error of the DC gain of the low-pass filter expressed as a percentage of some specific required value of DC gain.

As noted above, claims 1, 2 and 6 have been amended for clarification to recite the above described condition that the amount of percentage leakage of charge from the input capacitor (CI) during each phase 2 interval should be no greater than the maximum permissible amount of error of the DC gain of the filter, with that maximum permissible amount of error being no greater than 3%.

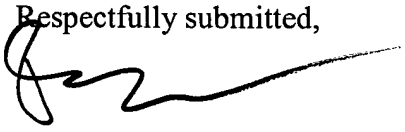
Thus, as can be understood from a review of the timing diagram of Fig. 8 of the present application, in a prior art switched capacitor filter operation, the switching elements have been controlled such that the above-described phase 2 interval has the same duration as the preceding and succeeding phase 1 interval and phase 3 interval leading to the disadvantages described in the applicants' specification. The prior art simply does not teach or imply that such a type of switched capacitor filter could be configured for operating at very low frequencies as described in the present application. Contrary to the Examiner's assertion, the claimed operation, which achieves a much shorting phase 2 interval than previously possible, satisfies a long felt need in the art based on the criticality of, *inter alia*, the claimed timing and switching operations.

Accordingly, a *prima facie* case of obviousness has not properly been established in that the Examiner admits that Figure 7 fails to teach or suggest all the claimed features as required. Applicants have shown that the claimed features involve critical timing issues to solve long felt needs and therefore are allowable. It is respectfully requested that the rejection of claims 1-7 be reconsidered and withdrawn.

In view of the foregoing, the applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



Robert L Scott, II
Reg. No. 43,102

Posz Law Group, PLC
12040 South Lakes Drive, Suite 101
Reston, VA 20191
Phone 703-707-9110
Fax 703-707-9112
Customer No. 23400